# PRODUCT SPECIFICATION

## MODEL: MTF055FD08A-V1

<◇> PRELIMINARY SPECIFICATION

<◆> APPROVAL SPECIFICATION

| CUSTOMER |
| --- |
| |
| **APPROVED BY** |
| |
| DATE: |

| DESIGNED | CHECKED | APPROVED |
| --- | --- | --- |
| LCM研发 2021.10.11 Qin | LCM研发 2021.10.11 YGP | LCM研发 2021.10.11 Edward |

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## 1. History Version

| Sample version | Doc. version | Date | Description | Modify |
|---|---|---|---|---|
| V00 | V00 | 2020-11-11 | First issue | LW |

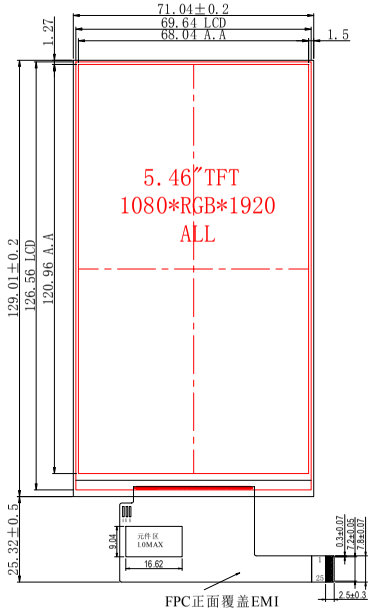
## 2. Mechanical Description

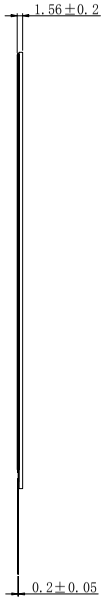
| Name | Content | Unit |
|---|---|---|
| Outline Size | 71.04 (W) * 129.01 (H) * 1.56(T) | mm |
| Module size | 5.46 (A.A) | inch |
| Resolution | 1080(RGB)* 1920 Pixels | - |
| Viewing size | 68.04(W) * 120.96(H) | mm |
| Pixel size | 0.063 * 0.063 | mm |
| LCD Type | TFT (16.7M)/ Transmissive | - |
| Viewing Angle | ALL | - |
| Driver IC | ILI7807D | - |
| Backlight Type | 7 Serial 2 Parallel | - |
| Interface Type | 4 LINE MIPI | - |

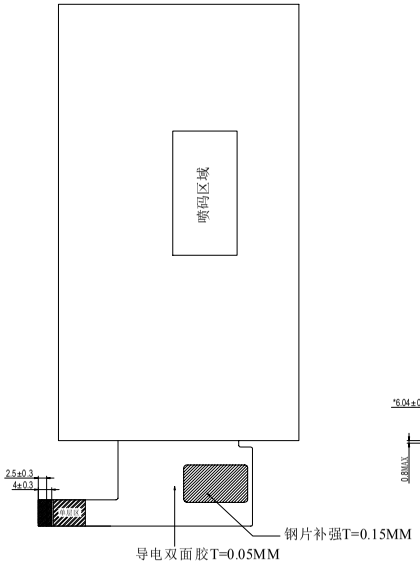
| 尺寸区域 | 允许公差 |
|---|---|
| L<=6.0 | ±0.10 |
| L>6.0 | ±0.15 |
| Angle | ±1° |

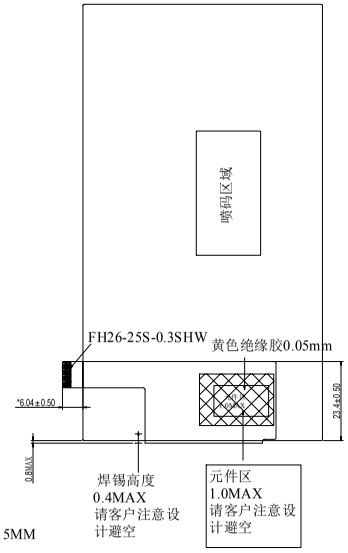
| 版本 | 日期 | 修改人 | 修改原因 | 修改内容 |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |

| | |
|---|---|
| 1 | LEDK |
| 2 | LEDA |
| 3 | LCD_ID |
| 4 | GND |
| 5 | D0N |
| 6 | D0P |
| 7 | GND |
| 8 | D1N |
| 9 | D1P |
| 10 | GND |
| 11 | CLKN |
| 12 | CLKP |
| 13 | GND |
| 14 | D2N |
| 15 | D2P |
| 16 | GND |
| 17 | D3N |
| 18 | D3P |
| 19 | GND |
| 20 | NC |
| 21 | GND |
| 22 | RESET |
| 23 | PWM |
| 24 | ID/VCC |
| 25 | VCC |



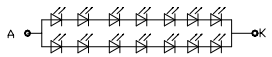




FPC弯折示意图

FPC弯折出货

NOTES:
1. DISPLAY TYPE:5.5″,LTPS SFT,
2. DISPLAY MODE:IPS NORMALLY BLACK
3. VIEWING DIRECTION: all O'clock
4. OPERATING TEMP:-20° C~70° C
STORAGE TEMP : -30° C~80° C
5. RoHS COMPLIANT.




IF=40MA, VF=21±2.1V

BRIGHTNESS:300cd/㎡ TYP

| 正式图 | | | | | |
|---|---|---|---|---|---|
| REV 版本 | A1 | PART No. 料号 | MTF055FD08A-V1 | | |
| SCALE 比例 | 1:1 | DESCRIPTION 品名 | | | |
| 第三视角 | | MATERIAL 材质 | / | APPROVED BY 核准 | CHECKED BY 审核 | DRAWN BY 绘图 |
| | | COLOR 颜色 | UNIT 单位 mm | | | |
| | | DATE 日期 | 2021-09-07 | | | LW |

## 4. Interface Definition

| PIN NO. | PIN Name | Function Description |
|---|---|---|
| 1 | LEDK | Cathode pin of backlight |
| 2 | LEDA | Anode pin of backlight |
| 3 | LCM_ID | NO CONNECT |
| 4 | GND | Ground |
| 5 | MIPI_D0N | MIPI-DSI Data0 differential signal input pins. |
| 6 | MIPI_D0P | MIPI-DSI Data0 differential signal input pins. |
| 7 | GND | Ground |
| 8 | MIPI_D1N | MIPI-DSI Data1 differential signal input pins. |
| 9 | MIPI_D1P | MIPI-DSI Data1 differential signal input pins. |
| 10 | GND | Ground |
| 11 | MIPI_CN | MIPI-DSI CLOCK differential signal input pins |
| 12 | MIPI_CP | MIPI-DSI CLOCK differential signal input pins |
| 13 | GND | Ground |
| 14 | MIPI_D2N | MIPI-DSI Data2 differential signal input pins. |
| 15 | MIPI_D2P | MIPI-DSI Data2 differential signal input pins. |
| 16 | GND | Ground |
| 17 | MIPI_D3N | MIPI-DSI Data3 differential signal input pins. |
| 18 | MIPI_D3P | MIPI-DSI Data3 differential signal input pins. |
| 19 | GND | Ground |
| 20 | NC | NC |
| 21 | GND | Ground |
| 22 | RESET | The external reset input |
| 23 | PWM | NC |
| 24 | IOVCC | TYP: 1.8V/2.8 V |
| 25 | VCC | TYP: 2.8V |

# 5. Interface Timing：

## 5.1 Reset Timing

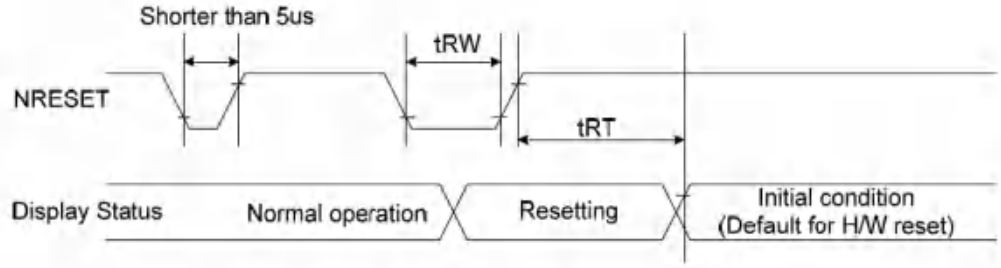



**Figure 102 Reset Timing**

**Table 41 Reset Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | tRW | Reset pulse duration | 10 | | us |
| | tRT | Reset cancel | | 5(note 1,5) | ms |
| | | | | 120 (note 1,6,7) | ms |

## 5.2 DSI DC Characteristics

### 5.2.1 DC characteristics for Power Lines

| Item | Symbol | Condition | Min. | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| **Power & Operation Voltage** | | | | | | | |
| Analog operating voltage | VCI | - | 2.5 | 2.8 | 3.3 | V | |
| Logic operating voltage | DPHYVCC | - | 1.65 | 1.8 | 3.3 | V | |
| Logic operating voltage | IOVCC | - | 1.65 | 1.8 | 3.3 | V | Note1,2 |
| Logic High level input voltage | VIH | - | 0.7*IOVCC | | IOVCC | V | Note1 |
| Logic Low level input voltage | VIL | - | -0.3 | | 0.3*IOVCC | V | Note1 |
| Logic High level output voltage FTE, FTE1, LEDPWM VSOUT,HSOUT, | VOH | IOH = -1.0mA | 0.8*IOVCC | | IOVCC | V | Note1 |
| Logic Low level output voltage FTE, FTE1, LEDPWM VSOUT,HSOUT, | VOL | IOL = +1.0mA | 0 | | 0.2*IOVCC | V | Note1 |
| Driver Supply Voltage | - | [VGH-VGL] | 11 | - | 31 | V | |
| **VCOM Operation** | | | | | | | |
| DC VCOM Amplitude Voltage | VCOM | - | -2.000 | - | 2.000 | V | Note3 |
| **Source Driver** | | | | | | | |
| Positive Source Output Range | VSOUT | - | 0.3 | - | GVDDP | V | Note4 |
| Negative Source Output Range | VSOUT | | GVDDN | - | -0.3 | | |
| Positive Gamma Reference Voltage | GVDDP | - | 3.0 | - | 6 | V | Note5 |
| Negative Gamma Reference Voltage | GVDDN | - | -6 | - | -3.0 | V | Note5 |
| Source Output Setting Time | Tr | Below with 99% precision | - | 1.5(TBD) | 1.6(TBD) | us | Note3,4 |
| Output Deviation Voltage (Source Output channel) | Vdev | Sout>=4.2V Sout<=0.8V | - | - | 30(TBD) | mV | Note3 |
| | | 4.2V>Sout>0.8V | - | - | 20(TBD) | mV | - |
| Output Offset Voltage | VOFFSET | - | - | - | 35(TBD) | mV | Note3 |
| **Booster Operation** | | | | | | | |
| VCL Voltage | VCL | - | TBD | | TBD | V | Note6 |
| Gate Driver High Voltage | VGHO | - | 6 | - | 13.0 | V | Note7 |
| Gate Driver Low Voltage | VGLO | - | -4 | - | -11 | V | Note8 |
| **Standby mode current consumption** | | | | | | | |
| Sleep In Mode | I(IOVCC SLP IN) | Ta = 25°C VCI=2.8V IOVCC=1.8V | - | (TBD) | (TBD) | uA | |
| | I(Vsp SLP IN) | | - | (TBD) | (TBD) | uA | |
| | I(Vsn SLP IN) | | - | (TBD) | (TBD) | uA | |
| Deep Standby Mode | I(IOVCC SLP IN) | | - | (TBD) | (TBD) | uA | |
| | I(Vsp SLP IN) | | - | (TBD) | (TBD) | uA | |
| | I(Vsn SLP IN) | | - | (TBD) | (TBD) | uA | |

### 5.2.2 DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode whe

LP-RX, LP-CD or LP-TX is mentioned on the condition column.

| Parameter | Symbol | Condition | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Logic High level output voltage | $V_{OH}$ | $I_{OUT}$=-1mA, Note 2 | 0.8 $V_{IOVCC}$ | - | $V_{IOVCC}$ | V |
| Logic Low level output voltage | $V_{OL}$ | $I_{OUT}$=1mA, Note 2 | 0.0 | - | 0.2$V_{IOVCC}$ | V |
| Logic High level input voltage | $V_{IHLPCD}$ | LP-CD, Note 3 | 450 | - | 1350 | mV |
| Logic Low level input voltage | $V_{ILLPCD}$ | LP-CD, Note 3 | 0.0 | - | 200 | mV |
| Logic High level input voltage | $V_{IHLPRX}$ | LP-RX (CLK, D0 ,D1), Note 3 | 880 | - | 1350 | mV |
| Logic Low level input voltage | $V_{ILLPRX}$ | LP-RX (CLK, D0 ,D1), Note 3 | 0.0 | - | 550 | mV |
| Logic Low level input voltage | $V_{ILULPRXLP}$ | LP-RX (CLK ULP mode), Note 3 | 0.0 | - | 300 | mV |
| Logic high level output voltage | $V_{OHLPTX}$ | LP-TX (D0), Note 3 | 1.1 | - | 1.3 | V |
| Logic Low level output voltage | $V_{OLLPTX}$ | LP-TX (D0), Note 3 | -50 | - | 50 | mV |
| Logic High level input current | $I_{IH}$ | LP-CD, LP-RX, Note 3 | - | - | 10 | uA |
| Logic Low level input current | $I_{IL}$ | LP-CD, LP-RX, Note 3 | -10 | - | - | uA |

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. LEDPWM · FTE · FTE1 · VSOUT · HSOUT
3. DSI High Speed mode is off

### 5.2.3 DC Characteristics for DSI HS mode

| Parameter | Symbol | Condition | Specification | | | Unit |
|---|---|---|---|---|---|---|
| Input Common Mode Voltage for Clock | $V_{CMCLK}$ | DSI-CLK+/- Note 2, Note 3 | 70 | - | 330 | mV |
| Input Common Mode Voltage for Data | $V_{CMDATA}$ | DSI-Dn+/- Note 2, Note 3, Note 5 | 70 | - | 330 | mV |
| Common Mode Ripple for Clock Equal or Less than 450MHz | $V_{CMRCLKL450}$ | DSI-CLK+/- Note 4 | -50 | - | 50 | mV |
| Common Mode Ripple for Data Equal or Less than 450MHz | $V_{CMRDATAL450}$ | DSI-Dn+/- Note 4, Note 5 | -50 | - | 50 | mV |
| Common Mode Ripple for Clock More than 450MHz (peak sine wave) | $V_{CMRCLKM450}$ | DSI-CLK+/- | - | - | 100 | mV |
| Common Mode Ripple for Data More than 450MHz (peak sine wave) | $V_{CMRDATAM450}$ | DSI-Dn+/- Note 5 | - | - | 100 | mV |
| Differential Input Low Level Threshold Voltage for Clock | $V_{THLCLK-}$ | DSI-CLK+/- | -70 | - | - | mV |
| Differential Input Low Level Threshold Voltage for Data | $V_{THLDATA-}$ | DSI-Dn+/- Note 5 | -70 | - | - | mV |
| Differential Input High Level Threshold Voltage for Clock | $V_{THHCLK+}$ | DSI-CLK+/- | - | - | 70 | mV |
| Differential Input High Level Threshold Voltage for Data | $V_{THHDATA-}$ | DSI-Dn+/- Note 5 | - | - | 70 | mV |
| Single-ended Input Low Voltage | $V_{ILHS}$ | DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5 | -40 | - | - | mV |
| Single-ended Input High Voltage | $V_{IHHS}$ | DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5 | - | - | 460 | mV |
| Differential Termination Resistor | $R_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- Note 5 | 80 | 100 | 125 | Ω |
| Single-ended Threshold Voltage for Termination Enable | $V_{TERM-EN}$ | DSI-CLK+/-, DSI-Dn+/- Note 5 | - | - | 450 | mV |
| Termination Capacitor | $C_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6 | - | - | 60 | pF |

Note:

1. Ta = -30℃ to 70℃ (to +85℃ no damage), IOVCC = 1.65 to 1.95V
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0,1,2,3
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

## 6. Absolute Maximum Ratings：

| Name | symbol | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| Operation Temperature | TOP | -20 | - | 70 | ℃ |
| Storage Temperature | TST | -30 | - | 80 | ℃ |

## 7. DC Characteristics

| Name | Symbol | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| Logical Voltage | VDD | 2.5 | 2.8 | 3.3 | V |
| Input High Voltage | VIH | 0.8IOVCC | - | IOVCC | V |
| Input Low Voltage | VIL | -0.3 | - | 0.2IOVCC | V |
| Output High Voltage | VOH | 0.8IOVCC | - | - | V |
| Output Low Voltage | VOL | - | - | 0.2IOVCC | V |
| Current Consumption | IDD | - | TBD | - | mA |

## 8. Blacklight：

| Name | Min | Type | Max | Unit |
|---|---|---|---|---|
| Current | 30 | 40 | - | mA |
| Voltage | 19.6 | 21.7 | 23.8 | V |
| luminance | 250 | 300 | - | $CD/M^2$ (Note1) |
| Luminance uniformity | 75% | 80% | - | (Note2) |
| X Color Coordinates | | | | - |
| Y Color Coordinates | | | | - |

Note1: This luminance is tested with assembling the LCD.
Note2: Definition of Luminance Uniformity.

Active area is divided into 9 measuring areas (Refer to Fig. 4-4 ).Every measuring point is placed at the center of each measuring area.

$$Luminance\ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L--------Active area length W------ Active area width

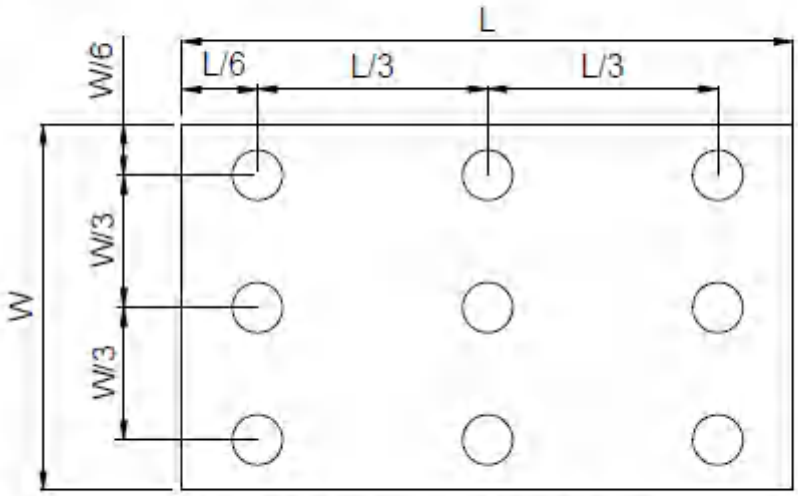


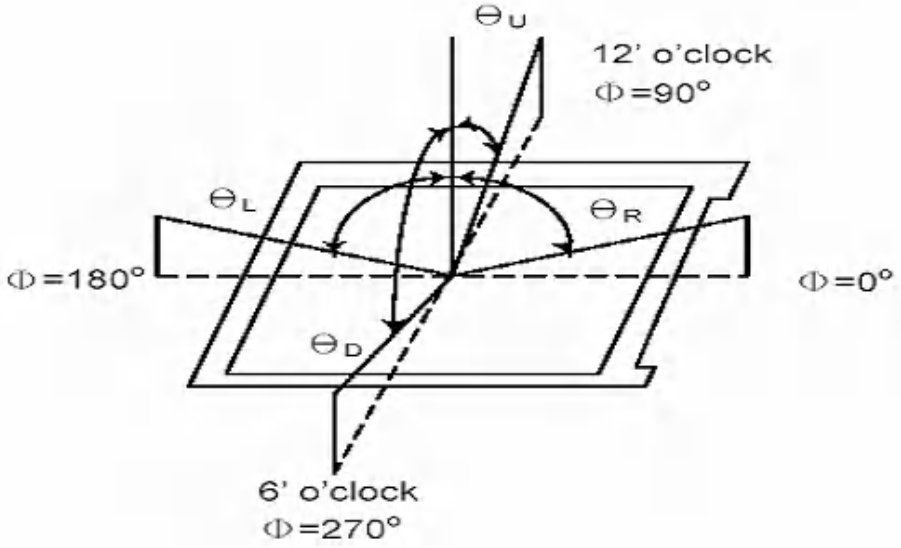

Fig. 4-4 Definition of measuring points

$B_{max}$: The measured maximum luminance of all measurement position.
$B_{min}$: The measured minimum luminance of all measurement position.

## 9. Optical Specification

| Name | Symbol | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| Transmittance rate | T(%) | - | 4 | - | % |
| Contrast ratio | C/R | 700 | 1000 | - | - |
| Response time | Tr+Tf | - | 45 | - | ms |
| Viewing Angle | θ U | 80 | 85 | - | degree （C/R>10） |
| | θ D | 80 | 85 | - | |
| | θ L | 80 | 85 | - | |
| | θ R | 80 | 85 | - | |

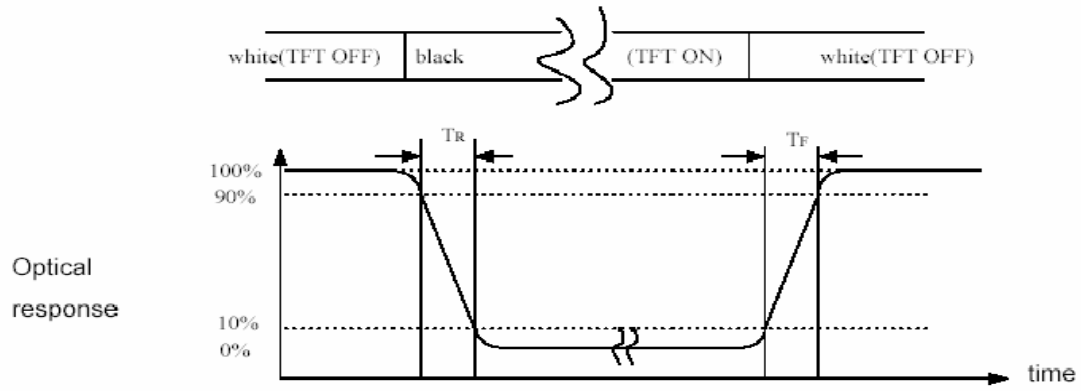
*Viewing angle description:




*Contrast rate description(CR) :
Tested in the center of the LCM panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

*Response time description : Sum of TR and TF



## 10. Reliability testing：

*One single product test for only one item.

* Judgment after test: keep in room temperature for more than 2 hours.

- Current consumption < 2 times of initial value

- Contrast > 1/2 initial value
- Function: work normally

## 11. Inspection Standard

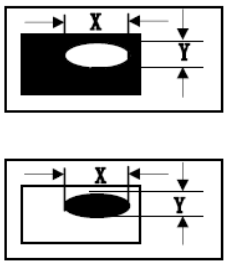
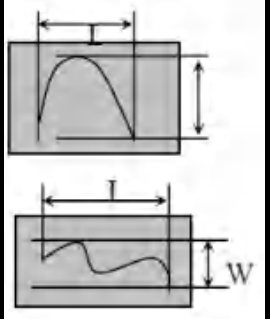
**11.1 Defect Defination**

| Item No | Name | Condition | Remark |
|---|---|---|---|
| 1 | High temperature Operating | 70° C , 48Hours | Finish product (With polarizer) |
| 2 | Low temperature Operating | -20° C , 48 Hours | Finish product (With polarizer) |
| 3 | High temperature Storage | 80° C , 48 Hours | Finish product (With polarizer) |
| 4 | Low temperature Storage | -30° C , 48 Hours | Finish product (With polarizer) |
| 5 | High temperature & humidity Storage | 60° C , 90%RH, 48 Hours | Finish product (With polarizer) |
| 6 | Thermal Shock Storage(No operation) | -20° C , 30min.<=> 70° C , 30min. 10 Cycles | Finish product (With polarizer) |
| 7 | ESD test | Voltage:+4KV R:330 ohm,C:150pF Air discharge,10 times | Finish product (With polarizer) |
| 8 | Vibration test | 10 => 55 =>10 => 55 => 10 Hz, within 1 minute;Amplitude:1.5mm. 15 minutes for each Direction ( X,Y,Z ) | Finish product (With polarizer) |
| 9 | Drop test | Packed, 60CM free fall 6 sides, 1 corner, 3edges | Finish product (With polarizer) |

**11.2 Standard**

| No. | Defect Class | Defination | Content |
|---|---|---|---|
| 1 | 重缺陷（MA） | 影响显示的功能缺陷 | 短路、断路、缺划、大电流、视角错、漏液、显示不清等 |
| | | 严重外观缺陷 | 产品尺寸不符、漏部品等 |
| 2 | 轻缺陷（MI） | 不影响产品功能，但对产品外观有影响 | 反黑 / 反白点、偏光片缺陷、针孔、污点 |

| No. | Item | Inspection Standard | Classification of defects |
|---|---|---|---|
| 1 | 显示状态 | 不显、显示乱码、多划、少划、少画面、视角错、闪烁等均不允许 | 重缺陷 |
| | | 无法用文字描述的现象，必要时制定限度样板进行参考。如：显示不均、显示浓淡、斜纹等 | |
| | | 显示的颜色效果参照开发、工程样品或按限度样板判定 | |
| | | 画面切换过程中可见(但非画异)之不良现象(暂停画面时不良现象不可见)不作管控，客户有特殊要求时依客户要求； | 轻缺陷 |
| | | 仅点背光不显示画面下可见不良现象（但显示画面时不良现象不可见)不作管控，客户有特殊要求时依客户要求； | 轻缺陷 |
| 2 | 背光 | LED 灯不亮或闪烁不稳定不允许 | 重缺陷 |
| | | 背光电流：超出规格范围不允许 | |
| | | 亮眼、漏光：进入 LCD 的 A、B 区不允许，必要时按限度样板做判定 | 轻缺陷 |
| | | 背光颜色：根据样品、规格书判定 | 轻缺陷 |
| | | 亮度与发光均匀度参照开发、工程或限度样板判定 | 轻缺陷 |

| No. | Item | Inspection Standard | | | Classification of defects |
|---|---|---|---|---|---|
| 3 | 显示黑点 白点 针孔 | 直径（Φ=（X+Y）/2） | 允收数 | 图示 | 轻缺陷 |
| | | Φ≤0.1 （密集不可） | 不计 |  | |
| | | 0.1<Φ≤0.15 [注2] | 2 | | |
| | | 0.15<Φ≤0.2 | 1 | | |
| | | Φ>0.2 | 0 | | |
| | | 注1. 包括：黑点、白点、针孔、异物。<br>注2. 整个产品不允许超过2个点,且间距必须在10mm以上。 | | | |
| 4 | 显示黑线 白线 | 尺 寸（L：线长；W：线宽） | 允收数 | 图示 | 轻缺陷 |
| | | L 不计 W<0.03（密集不可） | 不计 |  | |
| | | L≤2 0.03≤W≤0.05 [注 2] | 2 | | |
| | | L 不计 W>0.05 | 以点判断 | | |
| | | 注1. 包括：显示黑线、白线、线状异物。<br>注2. 单个产品不允许超过2个线状缺陷，且缺陷距离必须大于10mm以上。 | | | |
| 5 | 触摸屏 | 点击触摸屏测试点画面无转换不允许 | | | 重缺陷 |

## 12. Precaution

### 12.1 Handling

(1) Protect the panel from static, it may cause damage to the CMOS Gate Array IC.

(2) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(3) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(4) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Don't use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(5) Pins of I/F connector shall not be touched directly with bare hands.

(6) Refrain from strong mechanical shock and / or any force to the panel. In addition to damage, this may cause improper operation or damage to the panel.

(7) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a B pencil lead.

(8) Wipe off water droplets or oil immediately. If you leave the droplets for a long time,staining and discoloration may occur.

(9) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

**12.2 Storage**

(1) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the panel with temperature from 0 to 35℃ and relative humidity of less than 70%.

(2) The panel shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

**12.3 Operation**

(1) The LCD shall be operated within the limits specified. Operation at values outside of these limits may shorten life, and/or harm display images.

(2) Do not exceed the absolute maximum rating value. (the supply voltage variation,Input voltage variation in part contents and environmental temperature and so on).Otherwise the panel may be damaged.

(3) If the panel displays the same pattern continuously for a long period of time, it can be the situation when the image" Sticks" to the screen.